Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of manufacturing an integrated circuit comprising:

providing a substrate, the substrate including a layer including germanium;

providing a gate structure above the substrate;

pre-cleaning the substrate using hydrofluoric acid after the step of providing a gate structure; and

pre-cleaning the substrate with an argon and hydrogen plasma after the step of pre-cleaning the substrate using hydrofluoric acid; and

siliciding the substrate.

2. (Currently Amended) The method of claim 1, wherein the step of pre-cleaning the substrate using hydrofluoric acid removes thermal oxide from the substrate and the step of pre-cleaning the substrate using an argon and hydrogen plasma removes thermal oxide remaining after the step of pre-cleaning the substrate using hydrofluouric acid ~~pre-cleaning utilizes a hydrogen argon plasma~~.

3. (Currently Amended) The method of claim 1, wherein the ~~pre-cleaning also utilizes an HF dip~~ step of pre-cleaning the substrate using an argon and hydrogen plasma utilizes a total gas pressure of approximately 100 Pa and a hydrogen flow rate of approximately 100 sccm.

4. (Currently Amended) The method of claim 1, ~~further comprising:~~ wherein the step of pre-cleaning the substrate using hydrofluoric acid comprises exposing the substrate to a wet bath.

5. (Original) The method of claim 1, wherein the gate structure includes a polysilicon conductor.

6. (Original) The method of claim 5, wherein the polysilicon conductor is pre-cleaned and silicided.

7. (Currently Amended) A method of pre-cleaning a top surface of an IC substrate before silicidation in a chamber, the method comprising:

exposing the IC substrate to hydrofluoric acid to remove native oxide from the IC substrate; and

providing a plasma including hydrogen in the chamber to remove native oxide from the IC substrate remaining after the exposure of the IC substrate to hydrofluoric acid.; ~~and~~

~~removing native oxide from the IC substrate.~~

8. (Currently Amended) The method of claim 7, ~~further comprising~~ wherein the step of exposing the IC substrate to hydrofluoric acid comprises providing a wet bath to reduce a thickness of the native oxide.

9. (Currently Amended) The method of claim 8, wherein the wet bath utilizes hydrofluoric acid and water.

10. (Currently Amended) The method of claim 8, wherein the chamber is a vacuum chamber and a metal layer is deposited on the IC substrate in the chamber after the ~~pre-clean step~~ after the steps of exposing the IC substrate to hydrofluoric acid and providing a plasma including hydrogen in the chamber.

11. (Original) The method of claim 10, wherein the thickness of the native oxide on the IC substrate is eliminated using the wet bath.

12. (Original) The method of claim 7, further comprising providing a silicide layer.

13. (Original) The method of claim 7, further comprising evacuating the chamber.

14. (Original) The method of claim 7, wherein the plasma includes argon.

15. (Original) The method of claim 7, wherein the IC substrate includes a germanium containing gate conductor.

16. (Original) The method of claim 7, wherein the chamber is part of a deposition tool.

17. (Currently Amended) A method of manufacturing a transistor on an integrated circuit, the method comprising:

providing a gate structure on a top surface of a strained silicon layer or a silicon germanium layer;

removing a native oxide material from the strained silicon layer or silicon germanium layer using a hydrofluoric acid wet bath;

providing a plasma including hydrogen and argon to remove [[a]] the native oxide material; and

siliciding the top surface.

18. (Original) The method of claim 17, further comprising utilizing hydrofluoric acid to remove a portion of the native oxide material before providing the plasma including hydrogen and argon.

19. (Original) The method of claim 18, wherein the siliciding is a nickel siliciding process.

20. (Original) The method of claim 19, wherein the top surface includes a silicon/germanium gate conductor.

Amendments to the Drawings:

The drawing sheets attached in connection with the above-identified application containing Figures 1-16 are being presented as a new formal drawing sheet or sheets to be substituted for the previously submitted drawing sheet or sheets. A separate Transmittal of Formal Drawings has been provided herewith.